Jerry Wu

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Education

The George Washington University, Washington, DC
8/2002 – 6/2008: Ph.D in Electrical and Computer Engineering
New York University, Polytechnic, Brooklyn, NY
9/94 - 6/96: M.S. in Electrical Engineering
Thesis Title: Architecture design of various shared-memory ATM switches
National Chiao Tung University, Hsinchu, Taiwan
8/89 - 6/93: B.S. in Control Engineering

Professional Experience

J2 Universe LLC., North Potomac, MD, 2009-present

Senior Director: Primary Nanotechnology research leader.

- Machine Learning with hardware enhancement for communication and medical products
- GPU with built-in AI engine
- Brainwaves EEG for brain-computer interface.
- DSP design for image, voice and data processing.
- CMOS MEMS technologies and application to mobile device RF design.
- High frequency DSP and RF design.
- Low power design for mobile device.
- Carbon NanoTubes (CNTs): application for NanoSolar cells, semiconductor, MEMS sensors, biomedical sensors.
- SAW filter and biomedical sensors with MEMS technologies.
- Low Power semiconductor implementation with CPF.
- Top-down ASIC-FPGA design methodology.
- Synopsys TeraMax ATPG, Cadence Encounter, DRC, LVS, and P&R
- Modeling of VLSI SOC
- Project implementation on Altera and Xilinx FPGA.

Hughes Network Systems, Inc (HNS), Maryland, 1998 - 2009

Principal Engineer: Responsible for all development aspects of complex System-on-Chip ASICs for fixed and mobile communications systems, lead a highly skilled engineering team to deliver quality and cost effective ASICs.

- Manage the ASIC development process through complete product lifecycle including specification, development of detail designs, verification and physical design.
- SOC verification using SystemC, System Verilog, Specman or ESL tools.
- Low power design, Modem development, high speed interfaces such as DDR2, PCI express, Gigabit Ethernet, ARM processors and peripherals, AHB/AXI bus architectures.

Principal Engineer: Responsible for complex FPGA/ASIC and PCB module design for HNS ATM Enterprise Network Switch, SpaceWay Satellite Terminal, ground-based beam forming (GBBF) system, and 3G baseband processor.

- Lead the development of the low power architecture of the 3G UMTS standard baseband processor (Oberon). Oberon ASIC enables wireless mobile devices to communicate over the satellite portion of TerreStar's network
  - Lead the design of the power management architecture and implementation.
  - Lead the development of baseband system clock scaling for cellular phone low power design.
  - Power mode simulation using common power format (CPF) and Cadence Conformal Low Power (CLP).
- Lead the development of Satellite Base Station Subsystem (S-BSS) and air interface protocol for ICO and Terrestar Networks, Inc., including a novel ground-based beam forming (GBBF) subsystem which is a key component of its integrated satellite and terrestrial mobile network.
  - Lead the FPGA development environment, board-level and system-level development environment.
  - FPGA and GBBF system development process and training for team members.
  - DVT and satellite subsystem high-level integration test.
- Lead design of the 2nd generation network processor of SpaceWay Satellite Terminal.

- Performed performance analysis and architected/designed enhancement to improve system latency/performance in the chip.
- Lead the verification team and developed the test-plan and performed random based verification by using verisity e-language.
- Performed physical design and Floorplanning by using Magma tools and worked with back-end fabrication company (freescale).
- Developed timing constraints for synthesis and PrimeTime.
- Performed formal verification and gate-level ECO.
- Experience in building top-level chip simulation model and system regression tests.
- Developed DVT methodology and provided lab debug user manual.
- Debug and identify fails in the Lab.

- Initial designer of the Copernicus system design and performance analysis.
  The Copernicus ASIC is a network processor of SpaceWay Satellite Terminal. (7+ million gates)
  Responsibilities:
  - Responsible for the Up-link and down-link packet processor top-level design and system performance analysis.
  - System functional and performance analysis by using SystemC.
  - In charge of the Copernicus on chip system processor: Xtensa processor evaluation and performance testing.
  - In charge of the Copernicus on chip system bus: Sonics' SiliconBackplane evaluation and testing.
  - In charge of the Copernicus on chip system DDR controller IP evaluation, performance analysis and testing.
  - In charge of the Copernicus on chip PCI controller IP evaluation, performance analysis and testing.
  - Experience in running the entire Magma flow from RTL through GDS II
  - Familiarity with Magma back-end flow in floorplanning, Place & Route.
  - Performed formal verification.
  - Held the ASIC ISO and FSO reviews.
- Lead designer of the Satellite Terminal ASIC SSC (System Service Controller) sub-module.
  The SSC is a system queuing processor which support global inqueue, dequeue, system memory sharing and arbitration between eight of system processors.
  Responsibilities:
  - Functional model by using SystemC.
  - Block level design and RTL coding
  - Block level verification and top level random based verification by using Verisity e language.
  - FPGA implementation for satellite emulation board.
  - Top-down ASIC implementation: synthesis, formality verification, I/O timing/constrain analysis.
  - System DVT and lab debugging.
- Lead designer of the HNS BX5000 ATM Switch 8 Port T3/E3 UNI PHY Module with Redundancy Circuit.(HNS Patent)
  The T3/E3 PHY Daughter Card is a PHY layer interface card that receives/transmits 8 ports of T3/E3 ATM traffic and delivers it to the Multi-Service Physical Interface Module (MSPHY) through 2 UTOPIA ports.
  Responsibilities:
  - Developing the specifications and technical requirements
  - System integration, board level design, control FPGA design, Function Verification Test, Design Verification Test and product support
  - FPGA (XC4062XLA-BG432) design for control circuit by Verilog
  - 14 layers DS3/E3 PHY module Schematic drawing, PCB Design, critical signal routing
  - DVT and ATM Switch system integration testing.
  - Board level simulation using Mentor Graphic Quick-Sim, Cadence Verilog XL

University of Maryland, College Park, 2016-present

Adjunct Professor / Lecturer:
- MSML642: Robotics
- MSML640: Computer Vision
- MSML605: Computing Systems for Machine Learning
- ENEE459F: Advanced Laboratory in FPGA System Design
- ENEE459D: Advanced Laboratory of Digital SystemVerilog
- ENEE244: Digital Logic Design
- ENEE245: Digital Circuits and Systems Laboratory
- ENPM617: Compiler
- ENPM690: Robot Learning

George Washington University, Washington, DC, 2005-2017

ECE department
Adjunct Professor: Teach Design of VLSI circuit (ECE6213), advance VLSI design (ECE6214), ASIC Design Testing (ECE4150), VLSI Custom Design and Simulation (ECE4140)

- Schematic, Layout, DRC, LVS
- Synopsys TeraMax ATPG, Cadence Encounter, P&R
- GDS to MOSIS C5 Technology
- Low Power semiconductor implementation.
- Top-down ASIC-FPGA design methodology.
- Modeling of VLSI circuits using verilog HDL
- DSP design for image, voice and data processing.
- Introduction to logic design, simulation and synthesis by using Cadence and Synopsys tools.
- Project implementation on Altera DE-2 board and Xilinx Spartan-3A board.
- Brainwaves EEG for control system.

Lightcom Technologies Inc., Hazlet, NJ (9/95 – 7/98)
Design Engineer

- Design a shared-memory single chip ATM switch
- VHDL modeling of an ATM switch chip
- Develop an exhaustive testing strategy by using a mix of C programming and VHDL modeling for ATM switch chip
- Support training courses and technical transfer to customers
- Scalable IP switching router (scaled from 2.4 Gb/s to 25.6Gb/s)
- Design controller and pointer processing for per-flow queueing and weighted fair queueing to support Resource Reservation Protocol (RSVP) connections

New York University, Polytechnic, Brooklyn, NY (1/96 - 5/96)
Teaching Assistant: for VLSI-II

- VLSI design using VHDL, Design Architect, Mentor Graphic Led, Lsim, Autocell, Xilinx and ALTERA, FPGA(XC3020A, XC4003A)
- VLSI design using HP-0.8u technology

Research Project

- Design 16x16 Link-List Shared Memory ATM Switch
- Design shared memory application on SFQ
- Design the architecture and compile the VHDL codes with Autologic synthesisable constraint and simulate with Quicksim II
- Design ATM switch based on single-chip solution with UPC function

National Chiao Tung University, Hsinchu, Taiwan (6/93 – 8/94)
Lecturer: in Department of Computer Science & Information Engineering

- Lecture for ICE 8088F, 8088 Board emulation, HP 1650/51 Logic Analyzer
- Program 8086/8088 series relative chips, Super VGA card and Ethernet driver
- Program Ethernet and 93C65 Arcnet Boot ROM
- Maintain and setup 150 clients of Novell Netware.

National Chiao Tung University, Hsinchu, Taiwan (9/91 - 9/92)
Research Assistant: in Institute & Department of Control Engineering

- Development of FUZZY software by C program for college education
- Analyze and control the position and speed of floopy disk driver by assembler
- Program the controller of inverted pendulum by assembler
- Analysis of bicycle design based on system dynamics (received two awards)

Publication

- CMOS Mixer Design with Micromachined Input-Matching Circuits for Wireless Applications Design, *IEEE Circuits and Systems, ISCAS 2006.*
- Comparison of VCO Topology for Wideband Multi-Standard Applications, *IEEE Wireless and Microwave Technology Conference*, Dec. 2006, pp.1-4
- CMOS Micromachined Inductors with Structure Supports for RF Mixer Matching Networks, *IEEE Electron Device Lett.2008*
- Application of CMOS Micromachined Inductors With Structure Supports to Gilbert Mixer Matching Circuits, *IEEE Circuit and System, Aug. 2009*

- Non-cryogenic cooled MWIR with swap-limited carbon nanotubes, *Proc. SPIE 8058, Independent Component Analyses, Wavelets, Neural Networks, Biosystems, and Nanoengineering, 80580P (June, 2011)*
- Non-cryogenic cooled MWIR with swap-limited carbon nanotubes, *Proc. SPIE, (May, 2011)*
- A High Resolution Time-to-Digital Converter on FPGA for Time-Correlated Single Photon Counting, *55th Int'l Midwest Symposium on Circuits & Systems, (Aug, 2012)*.
- A NANO enhance to Moore's Law, *Proc. SPIE 8401, Independent Component Analyses, Compressive Sampling, Wavelets, Neural Net, Biosystems, and Nanoengineering*, *84010P (May, 2012)*
- Health sensor for human body by using infrared, acoustic energy and magnetic signature, *Proc. SPIE Independent Component Analyses*, (June, 2013)
- Future enhancements to 3D printing and real time production, Proc. SPIE *Independent Component Analyses, (June, 2014)*
- Brain order disorder 2nd group report of f-EEG, *Proc. SPIE (May, 2014)*
- Spatially revolved high density electroencephalography, Proc. SPIE, *Independent Component Analyses, (June, 2015)*
- Hardware enhance of brain computer interfaces, Proc. SPIE *Independent Component Analyses, (June, 2015)*

Summary

- Over 29 years hands on experience in RF MEMS, Nanotechnology semiconductor, ASIC, FPGA, PCB, and data communication system design and verification.
- Over 24 years in telecommunications and satellite communication industry.
- Completion of the full development cycle from technical specification to post development product support on several production projects.
- Excellent problem solving and lab debugging skills.
- Fast learner and good interpersonal communication skills.
- In depth knowledge of Nanotechnology, RF MEMS, ASIC, FPGA, Magma, Cadence CLP, CPF, Verilog HDL, VHDL, SystemC, Verisity, SystemVerilog, Synopsys, Synplicity Synplify, XILINX, ALTERA, VLSI, SONET, ATM network and related protocol, IEEE 802.3, Ethernet, T1/E1, T3/E3, TCP/IP, LAN/WAN, PCI, Intel i960 microprocessor, Xtensa Processor.

Skills

Machine Learning with hardware enhancement
Enhanced by FPGA platform, ML/AI with FPGA accelerator, Brainwaves EEG.
Nanotechnology
Carbon NanoTubes (CNTs), NanoSolar calls, Nanotechnology semiconductor, MEMS sensors, biomedical sensors, SAW filters for bio-sensor.
Low Power Design for Mobil Device
Cadence Conformal Low Power (CLP), common power format (CPF), power simulation.
VLSI System Design
CMOS technology, circuit design and layout, digital system design, FPGA, and standard cell.
FPGA Design
Fluent usage of FPGA Express, Design Manager, Floor Planner, Design Constrain editing.
PCB Board Design
Design up to 14 layers module using Mentor Graphic Design Architect
Networking
Ethernet, T1/E1, T3/E3, SONET, ATM Switch
Microprocessor System
ARM, Xtensa, Sonics SiliconBackplane, 8086/88 system, 8255, 8251, 8237, 8254, 8288 driver programming by using Assembler, 93C65 Arcnet control programming
Software

- SystemVerilog, Verilog, VHDL, SystemC, Verisity e language, Perl.
- Mentor Graphic IC Design Tools : Led, Lsim, DA, Dmgr, Autologic, Qvsim
- Magma ASIC design tools.
- OS/2, Linux, Unix, Windows O/S, Novell
- C, Assembler, Matlab, Pascal, HTML
- Photoshop, Pagemaker, Director, Premiere

Control System
PID controller, Sliding mode controller, FUZZY-integrated programmable of logic controller (FPLC)

Awards Received

- **Silver Prize,** National Chiao Tung University Research and Development Award
- **Best Award**, (10/93) The CIE (Chinese Institute of Engineers), Taiwan Engineering Students Research Paper Contest

Reference upon request